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NILANONT, YOUPAPORN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,111	OOI, TAKUYA	
	Examiner	Art Unit	
	YOUPAPORN NILANONT	2446	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. **Status of Claims:**

Claims 1-17 are pending in this Office Action.

Claims 1-17 are amended.

The objections to the title and to the minor informalities of the disclosure and the rejections under 35 U.S.C. 112 and 35 U.S.C. 101 are withdrawn based on applicant's amendments

Response to Arguments

2. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's invention as claimed:

Claim Construction

"information processing apparatus" cited in claim 1 and claims 3-17 is inconsistent with the specification and has been construed as either "synchronization master apparatus" cited on page 10 line 12 or "synchronization slave apparatus" cited on page 11 line 2;

"synchronization control data" cited in claims 1, 3-5, 7, 10-12, and 16-17 is inconsistent with the specification and has been construed as "synchronization control frame" as cited on page 14 line 19;

"generation means" cited in claims 1 and 5 is inconsistent with the specification and has been construed as “synchronization frame processing section 91” as cited on page 14 line 17;

“counter value” cited in claims 8, 9, 14, and 15 is inconsistent with the specification and has been construed as “MPEG packet counter value” as cited on page 14 line 27;

“transmission means,” “control data transmission means,” and “data transmission means” cited in claims 1, 5, 8, and 14 are inconsistent with the specification and have been construed as "network communication section 85" cited on page 14 line 23 and page 15 line 20, 25 since the "network communication section 85,” as described, transmits control frame to slave apparatuses;

“transmission resetting means” cited in claim 1 is inconsistent with the specification and has been construed as “counter resetting section 104” as cited on page 18 line 14;

"acquisition means” cited in claims 9 and 15 is inconsistent with the specification and has been construed as “counter value acquisition section 243” as cited on page 31 line 21-22;

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 4-5, 10-12 and 16-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The term "substantially" recited in claims 1 and 4 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

6. The term “immediately” recited in claims 1, 4-5, 10-12 and 16-17 is a relative term which renders the claim indefinite. The term "immediately" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and it would be reasonable for one of ordinary skill in the art to interpret the term “immediately” to have different ranges in time.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 4-6, 10-13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth (US 6199169) in view of Dworkin et al. (US 2003/0058893).

9. **Regarding claim 1,** Voth teaches a communications system (Voth, figure 1), comprising:

a first information processing apparatus (Voth, figure 6 “Master Node”, “master node 102a” Column 4 Line 40);

and a second information processing apparatus interconnected with said first information processing apparatus by a network (Voth, figure 6 “Slave Node", figure 1), whereby data is communicated between first information processing apparatus and said second information processing apparatus (Voth, “master node sends a SYNC message...to a slave node...slave node…returns the SYNC message to the master node…master node sends an INFO message to the slave node" Abstract);

said first information processing apparatus including:

a transmission clock counter that counts an internal transmission clock (Voth, figure 2 "time clock 212"),

generation means that generates, at a predetermined time, synchronization control data (Voth, “creating…INFO message” column 7 lines 48-49),

transmission means that transmits the synchronization control data to said second information processing apparatus (Voth, “sending an INFO message" column 7 line 39),

and transmission resetting means that resets said transmission clock counter upon the transmission of the synchronization control data

being completed (Voth, “Master node 102a applies the time changes and adjustments to its own time clock 212” column 15 lines 45-57 and column 16 line 1);

and said second information processing apparatus including (Voth, "slave nodes 102b-d" column 4 line 41):

a reception clock counter that counts an internal reception clock (Voth, “time clocks 212” column 5 lines 8-10), and

reception resetting means that resets said reception clock counter upon the receiving of the data being completed and the received data being determined to be the synchronization control data (Voth, “slave nodes 102b-d to set their time clocks to a specified value" column 4 lines 54-58).

Though Voth does not explicitly disclose data determining data determining means that determines whether or not data that is received by said second information processing apparatus is the synchronization control data, it is inherent that Voth system requires means to distinguish INFO message, which informs slave nodes to adjust their clocks, from the SYNC message and other messages received from the master node (Voth, column 5 lines 33-34 and 60-61 "distinguishes...from other message types").

However, Voth does not explicitly disclose that the transmission clock counter resets "immediately" after transmitting the INFO message and the reception clock

counter resets “immediately” after receiving the INFO message. However, the Voth reference does suggest that the INFO message includes a value telling everyone receiving the INFO message to reset at the scheduled time as indicated by the included value (Voth, column 8 lines 12-13, column 15 lines 55-56).

Conversely, Dworkin discloses a system where in the first device generates and transmits a signal to other devices and other device will reset their counter by loading a value upon receipt of a signal from the first device (Dworkin, paragraph [0009] 6th and 7th sentences).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have incorporated Dworkin’s synchronization teaching in Voth’s disclosure in order to make Voth’s small adjustment (Voth, column 4 line 16 "small adjustments are applied immediately") without having to add an extra flag or field in the INFO message sent and therefore reduce the size of control packet being sent.

10. **Regarding claim 2,** the way Voth reference determines whether the slave clocks lag or lead the master clock is obvious that all the clocks count values in the same range without having to explicitly state that said transmission clock counter and said reception clock counter count values in the same range. If the Voth's clock counters count values that are not in the same range, the result of Voth’s comparison will be meaningless in determining whether a slave clock lags or lead the master clock.

11. **Regarding claim 4,** Voth reference teaches a communications method in which data is communicated between a first information processing apparatus and a second

information processing apparatus which are interconnected by a network (Voth, figure 1 “102a-d” and “104”), said method comprising:

generating, at the first information processing apparatus, synchronization control data (Voth, “master node...by creating and sending an INFO message" column 7 lines 38-39 and "tells slave node 102 when to implement time changes and adjustments that are included in INFO message" lines 47-49);

transmitting the generated synchronization control data from the first information processing apparatus to said the second information processing apparatus (Voth, “master node…by creating and sending an INFO message” column 7 lines 38-39 and “an INFO message 500 should be sent to slave node” line 20); and

resetting a transmission clock counter that counts an internal transmission clock upon the transmission of the synchronization control data being completed (Voth, “Master node 102a applies the time changes and adjustments to its own time clock 212” columns 15-16 lines 45-57 and line 1); and

resetting, at the second information processing apparatus, a reception clock counter that counts an internal reception clock upon the receiving of the data being completed and the received data being determined to be the synchronization control data (Voth, “slave nodes 102b-d to set their time clocks to a specified value" column4 lines 54-58),

Though Voth reference does no explicitly disclose a communications method of determining, at the second information processing apparatus, whether

or not data that is received by the second information processing apparatus is the synchronization control data, it is inherent that the Voth system requires a step of distinguishing INFO message, which is used to inform slave nodes to adjust their clocks, and SYNC message from one other and from other message by checking for a flag in the data's header.

However, Voth does not explicitly disclose that the transmission clock counter resets "immediately" after transmitting the INFO message and the reception clock counter resets “immediately” after receiving the INFO message. However, the Voth reference does suggest that the INFO message includes a value telling everyone receiving the INFO message to reset at the scheduled time as indicated by the included value (Voth, column 8 lines 12-13, column 15 lines 55-56).

Conversely, Dworkin discloses a system where in the first device generates and transmits a signal to other devices and other device will reset their counter by loading a value upon receipt of a signal from the first device (Dworkin, paragraph [0009] 6th and 7th sentences).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have incorporated Dworkin’s synchronization teaching in Voth’s disclosure in order to make Voth’s small adjustment (Voth, column 4 line 16 "small adjustments are applied immediately") without having to add an extra flag or field in the INFO message sent and therefore reduce the size of control packet being sent.

12. **Regarding claim 5,** Voth reference teaches an information processing apparatus for transmitting/receiving data with another information processing apparatus connected thereto by a network (Voth, figure 1), comprising:

a transmission clock counter that counts an internal clock (Voth, figure 2 "time clock 212);

generation means that generates, at a predetermined time, synchronization control data that instructs a reset of a reception clock counter of said another information processing apparatus (Voth, “creating…INFO message” column 7 lines 38-39 and “tells slave node 102 when to implement time changes and adjustments that are included in INFO message" lines 47-49);

control data transmission means that transmits the synchronization control data to the another information processing apparatus (Voth, “sending an INFO message” column 7 line 39 and “an INFO message 500 should be sent to slave node” line 20); and

reset means that resets the transmission clock counter upon the transmission of the synchronization control data being completed (Voth, “Master node 102a applies the time changes and adjustments to its own time clock 212” columns 15-16 lines 45-57 and line 1).

However, Voth does not explicitly disclose resetting of clock "immediately". However, the Voth reference does suggest that the INFO message includes a value telling everyone receiving the INFO message to reset at the scheduled time as indicated by the included value (Voth, column 8 lines 12-13, column 15 lines 55-56).

Conversely, Dworkin discloses a system where in the first device generates and transmits a signal to other devices and other device will reset their counter by loading a value upon receipt of a signal from the first device (Dworkin, paragraph [0009] 6th and 7th sentences).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have incorporated Dworkin's synchronization teaching in Voth's disclosure in order to make Voth's small adjustment (Voth, column 4 line 16 "small adjustments are applied immediately") without having to add an extra flag or field in the INFO message sent and therefore reduce the size of control packet being sent.

13. **Regarding claim 6,** the way Voth reference determines whether the slave clocks lag or lead the master clock (Voth, column 2 lines 57-65) is obvious that all the clocks count values in the same range without having to explicitly state that clock counter counts values of the transmission clock counter are in the same range as clock counter values of the reception clock counter of said another information processing apparatus. If the Voth's clock counters count values that are not in the same range, the result of the comparison will be meaningless in determining whether a slave clock lags or leads the master clock.

14. **Regarding claim 10,** Voth teaches an information processing method for transmitting/receiving data between a first information processing apparatus and a second information processing apparatus connected to each other by a network (Voth, figure 6 "Master Node" and "Slave Node"), comprising:

generating, at the first information processing apparatus at a predetermined time, synchronization control data that instructs a reset of a reception clock counter of said second information processing apparatus (Voth, “master node…by creating…INFO message” column 7 lines 38-39 and “tells slave node 102 when to implement time changes and adjustments that are included in INFO message" lines 47-49);

transmitting the generated synchronization control data from the first information processing apparatus to the second information processing apparatus (Voth, “master node…sending an INFO message” column 7 line 39 and “an INFO message 500 should be sent to slave node” line 20); and

resetting, at the first information processing apparatus, a transmission clock counter that counts an internal clock upon the transmission of the synchronization control data being completed (Voth, “Master node 102a applies the time changes and adjustments to its own time clock 212” columns 15-16 lines 45-57 and line 1).

However, Voth does not explicitly disclose resetting of clock "immediately". However, the Voth reference does suggest that the INFO message includes a value telling everyone receiving the INFO message to reset at the scheduled time as indicated by the included value (Voth, column 8 lines 12-13, column 15 lines 55-56).

Conversely, Dworkin discloses a system where in the first device generates and transmits a signal to other devices and other device will reset their counter by loading a

value upon receipt of a signal from the first device (Dworkin, paragraph [0009] 6th and 7th sentences).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have incorporated Dworkin's synchronization teaching in Voth's disclosure in order to make Voth's small adjustment (Voth, column 4 line 16 "small adjustments are applied immediately") without having to add an extra flag or field in the INFO message sent and therefore reduce the size of control packet being sent.

15. **Regarding claim 11,** Voth and Dworkin reference teach all of its limitations as cited above in the rejection of claim 10 since claim 11 recites a processor encoded with program that performs all of claim 10 functions. Furthermore, Voth's devices are disclosed as computing devices that can compute times and other value and obviously have processor. Additionally, Dworkin's device is shown as having a CPU for performing its function in figure 2. Claim 11, therefore, is taught by the combination of Voth and Dworkin references.

16. **Regarding claim 12,** Voth teaches an information processing apparatus for transmitting/receiving data with another information processing apparatus connected thereto by a network (Voth, figures 1 and 6), the apparatus comprising:

a first clock counter that counts an internal clock (Voth, "time clocks 212" column 5 lines 8-10);

data determining means that determines whether or not data that is received from the another information processing apparatus is synchronization control data which instructs a reset of said first clock counter at the same time as

a reset of a second clock counter of said another information processing apparatus (Though Voth does not explicitly disclose data determining data determining means that determines whether or not data that is received by said second information processing apparatus is the synchronization control data, it is inherent that Voth system requires means to distinguish INFO message, which informs slave nodes to adjust their clocks, from the SYNC message and other messages received from the master node (Voth, column 5 lines 33-34 and 60-61 "distinguishes...from other message types")); and

reset means that resets said first clock counter upon the receiving of the data being completed and the received data being determined to be the synchronization control data (Voth, “slave nodes 102b-d to set their time clocks to a specified value" column 4 lines 54-58).

However, Voth does not explicitly disclose resetting of clock "immediately". However, the Voth reference does suggest that the INFO message includes a value telling everyone receiving the INFO message to reset at the scheduled time as indicated by the included value (Voth, column 8 lines 12-13, column 15 lines 55-56).

Conversely, Dworkin discloses a system where in the first device generates and transmits a signal to other devices and other device will reset their counter by loading a value upon receipt of a signal from the first device (Dworkin, paragraph [0009] 6th and 7th sentences).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have incorporated Dworkin’s synchronization teaching

in Voth's disclosure in order to make Voth's small adjustment (Voth, column 4 line 16 "small adjustments are applied immediately") without having to add an extra flag or field in the INFO message sent and therefore reduce the size of control packet being sent.

17. **Regarding claim 13,** the way Voth determines whether the slave clocks lag or lead the master clock (Voth, column 2 lines 57-65) is obvious that all the clocks count value in the same range without having to explicitly state that first clock counter counts values in the same range as said second clock counter of said other information processing apparatus. If Voth's clock values are not in the same range, the result of the comparison will be useless in determining whether a slave clock lags or leads the master clock.

18. **Regarding claim 16,** Voth teaches an information processing method, the method comprising:

counting an internal clock using a first clock counter (Voth, "time clocks 212" column 5 lines 8-10);

determining whether data received from an information processing apparatus is synchronization control data (Though Voth does not disclose any step of determining synchronization control data, it is inherent, as cited above, that Voth's slave nodes requires distinguishing received INFO message and SYNC message from each other and from other received message (Voth, column 5 lines 33-34 and 60-61 "distinguishes...from other message types")) which instructs, at the same time as a reset of a second clock counter of the information processing apparatus, a reset of the first clock counter (Voth, "time

changes and adjustments that are included in INFO message" column 7 lines 48-49, "Upon receipt, slave node…time clock 212 will be updated…implements time changes by setting its time clock" column 8 lines 6-14 and column 5 lines 6-10); and

resetting the first clock counter upon the receiving of the data being completed and the received data being determined to be synchronization control data (Voth, "slave nodes 102b-d to set their time clocks to a specified value" column4 lines 54-58).

However, Voth does not explicitly disclose resetting of clock "immediately". However, the Voth reference does suggest that the INFO message includes a value telling everyone receiving the INFO message to reset at the scheduled time as indicated by the included value (Voth, column 8 lines 12-13, column 15 lines 55-56).

Conversely, Dworkin discloses a system where in the first device generates and transmits a signal to other devices and other device will reset their counter by loading a value upon receipt of a signal from the first device (Dworkin, paragraph [0009] 6th and 7th sentences).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have incorporated Dworkin's synchronization teaching in Voth's disclosure in order to make Voth's small adjustment (Voth, column 4 line 16 "small adjustments are applied immediately") without having to add an extra flag or field in the INFO message sent and therefore reduce the size of control packet being sent.

19. **Regarding claim 17,** Voth and Dworkin reference teach all of its limitations as cited above in the rejection of claim 16 since claim 17 recites a processor encoded with program that performs all of claim 16 functions. Furthermore, Voth's devices are disclosed as computing devices that can compute times and other value and obviously have processor. Additionally, Dworkin's device is shown as having a CPU for performing its function in figure 2. Claim 17, therefore, is taught by the combination of Voth and Dworkin references.

20. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth (US 6199169) in view of Dworkin et al. (US 2003/0058893) as applied to claims 1 and 5 above, and further in view of Sato (US 6128318).

21. **Regarding claim 3,** the modified Voth teaches the communications system according to claim 1, but does not further disclose the counter determining means nor that the transmission means transmits control message when the counter is determined to be zero. The Voth's system send control message in update cycles. The time between each cycle is computed by the master node (Voth, column 10 lines 62-67).

Conversely, Sato teaches communications system wherein said first information processing apparatus further comprises

> counter determining means that determines whether or not a value of said transmission clock counter becomes zero;
>
> and if the value of said transmission clock counter is determined as to become zero by said counter determining means, said transmission means transmits said synchronization control data generated by said generation means

to said second information processing apparatus (Sato, "reset signal is regularly asserted at a prescribed rate that is preferably a multiple of one cycle...period required for a cycle timer to count from an initial value to its final value…initial value is typically zero" column 4 lines 19-25).

It would have been obvious to the person having ordinary skill in the art at the time the invention was made to utilize Sato's teaching in predetermining when to send each synchronization message in Voth's system in order to synchronize clocks of every node effectively without requiring an additional hardware to calculate and store Voth's predetermined period between update cycles.

22. **Regarding claim 7,** modified Voth reference teaches the information processing apparatus according to claim 5, but does not further disclose the counter determining means nor that the transmission means transmits control message when the counter is zero. The Voth's system send control message in update cycles. The time between each cycle is computed by the master node (Voth, column 10 lines 62-67).

Conversely, Sato teaches an apparatus comprising:

counter determining means that determines whether or not a value of said transmission clock counter becomes zero;

wherein if a value of said transmission clock counter is determined to be zero by said counter determining means, said control data transmission means transmits said synchronization control data generated by said generation means to said another information processing apparatus (Sato, "reset signal is regularly asserted at a prescribed rate that is preferably a multiple of one cycle...period

required for a cycle timer to count from an initial value to its final value…initial value is typically zero" column 4 lines 19-25).

It would have been obvious to the person having ordinary skill in the art at the time the invention was made to utilize Sato's teaching in predetermining when to send each synchronization message in Voth's system in order to synchronize clocks of every node effectively without requiring an additional hardware to calculate and store Voth's predetermined period between update cycles.

23. Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth (US 6199169) in view of Dworkin et al. (US 2003/0058893) as applied to claims 5 and 12 above, and further in view of Zdepski (US 5486864).

24. **Regarding claim 8,** modified Voth teaches the information processing apparatus according to claim 5, but does not disclose adding means that adds a counter value to the header. However Voth's master node does add a calculated value to the header of INFO message to indicate when the slave nodes should reset their clock to a value included in received INFO message.

Zdepski, on the other hand, teaches an apparatus comprising:

adding means that adds to a header of said data, based on a value of said clock counter (Zdepski, figure 1 "Format 12" "Counter 23" and "Latch 24"), a counter value indicating the timing at which said another information processing apparatus processes data (Zdepski, "count values are denoted presentation time stamps…included in the compressed video signal" column 3 lines 13-17); and

data transmission means that transmits to said another information processing apparatus said data to which said counter value added by said adding means (Zdepski, figure 1 "Modem 15" and column 3 lines 1-2).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have employed Zdepski synchronization method in Voth system where each apparatus has its own local clock in order to enable the master node ability to instruct the slave nodes to output same images simultaneously across all slave nodes.

25. **Regarding claim 14,** modified Voth teaches the information processing apparatus according to claim 12 wherein a header of the received INFO message includes a value indicating the time at which the slave nodes are scheduled to change their clocks to a value that is also included in the received INFO message. Voth does not explicitly disclose that this value is based on the value of the sender's clock counter.

However, Zdepski teaches the information processing apparatus that adds counter value to the header of packet before sending to the receiver to indicate when the receiver should process data (Zdepski, figure 1 "Format 12", "Counter 23", "Latch 24", "count values are denoted presentation time stamps…included in the compressed video signal" column 3 lines 13-17, figure 1 "Modem 15" and column 3 lines 1-2).

It would have been obvious to the person having ordinary skill in the art, at the time the invention was made, to have employed Zdepski synchronization means in Voth system where each apparatus has its own local clock in order to enable the master

node ability to instruct the slave nodes to output same images simultaneously across all slave nodes.

26. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth (6199169) in view of Dworkin et al. (US 2003/0058893) as applied to claims 5 and 12 above, and further in view of Nuber (5598415).

27. **Regarding claim 9,** modified Voth teaches the information processing apparatus according to claim 5, but does not disclose the acquisition means, time determining means and data processing means that perform specific tasks as cited in claim 9.

Conversely, Nuber teaches the information processing apparatus further comprising:

acquisition means that acquires a counter value, which indicates the timing at which data is processed, added by said another information processing apparatus (Nuber, column 5 lines 41-42, lines 15-20);

time determining means that determines whether or not a value of transmission clock counter reaches said counter value acquired by said acquisition means (Nuber, “means responsive to the extracted PTS…” column 5 lines 44-48); and

data processing means that processes said data if said time determining means determines that the value of said transmission clock counter reaches said counter value (Nuber, figure 4 “ISO Data Extractor 110” and column 10 lines 64-67).

It would have been obvious to the person having ordinary skill in the art at the time the invention was made to have applied means for extracting presentation time stamp taught by Nuber in Voth system in order to enable the slave node to display same images at the same time as other slave nodes.

28. **Regarding claim 15,** modified Voth teaches the information processing apparatus according to claim 12, but does not disclose the acquisition means, time determining means and data processing means that perform specific tasks as cited in claim 15.

Conversely, Nuber teaches the information processing apparatus further comprising:

acquisition means that acquires a counter value, which indicates a timing at which data is processed, from said another information processing apparatus (Nuber, column 5 lines 41-42, lines 15-20);

time determining means that determines whether or not a value of said first clock counter reaches the counter value (Nuber, "means responsive to the extracted PTS…" column 5 lines 44-48); and

data processing means that processes the received data when said time determining means determines that the value of said clock counter reaches said counter value (Nuber, figure 4 "ISO Data Extractor 110" and column 10 lines 64-67).

It would have been obvious to the person having ordinary skill in the art at the time the invention was made to have applied means for extracting presentation time

stamp taught by Nuber in Voth system in order to enable the slave node to display same images at the same time as other slave nodes.

REMARKS

Applicant has presented amendments to the claims.

The Applicant Argues:

that the relied on sections of Voth does not disclose or suggest resetting of a transmission clock counter and the resetting of clocks as disclosed by relied on references does not happen immediately upon completion of synch transmission or reception.

In response, the examiner submits:

that the relied on sections of Voth does suggest a master clock reset (Voth, "master node 102a applies the time changes and adjustments to its own time" column 15 lines 55-56). However, the immediate effect of the clock reset was not claimed as part of the originally filed claims, thus required the examiner to rely on a new prior art.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUPAPORN NILANONT whose telephone number is (571) 270-5655. The examiner can normally be reached on Monday through Thursday and alternate Friday at 8:30 AM - 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey C. Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. N./

Examiner, Art Unit 2446

/Jeffrey Pwu/
Supervisory Patent Examiner, Art Unit 2446